Paper No. 11

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TAKAYUKI NIUYA

Appeal No. 2001-0046
Application 08/971,014[1]

ON BRIEF

Before HAIRSTON, GROSS and SAADAT, Administrative Patent Judges.

SAADAT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the Examiner's final rejection of claims 1-16. Claims 17-23 are withdrawn from consideration as being drawn to a non-elected invention.

We reverse.

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[1] Application for patent filed November 14, 1997.

BACKGROUND

Appellant's invention is directed to a method for fabricating contacts for formation of stacked capacitors in a layered semiconductor structure such as a DRAM circuit. The method includes forming a contact region in the semiconductor material structure and forming a conductive layer in a cavity characterized by a bottom portion formed of a first material and sides formed of a second material (specification, page 3). According to Appellant, higher etch depth may be achieved for forming small holes in thick layers of oxide (id.).

Representative independent claim 1 is reproduced as follows:

> 1. A method for fabricating an integrated circuit, comprising the steps of:
>
> forming a contact region in a semiconductor material structure;
>
> covering said semiconductor material structure, excluding said contact region, with a first material;
>
> covering said first material and said contact region with a layer of a second material;
>
> removing portions of said layer of second material and exposing said contact region, said removal of said portions of said layer of second material and exposing said contact region forming a cavity characterized by a bottom of an upper portion being said first material and sides of said upper portion being second material; and
>
> forming a conductive layer in said cavity to contact said contact region and conform to said bottom and sides.

The Examiner relies on the following references in rejecting the claims:

Takaishi	5,801,079 (effectively filed Jul. 28, 1995)	Sep. 1, 1998
Sekiguchi et al. (Sekiguchi)	5,933,724 (filed Aug. 26, 1996)	Aug. 3, 1999

Claims 1-16 stand rejected under 35 U.S.C. § 103 as being unpatentable over Sekiguchi and Takaishi.

We note that claim 8 was also rejected under the second paragraph of 35 U.S.C. § 112 as set forth in the final rejection (Paper No. 7, mailed January 6, 2000), which was neither included nor argued in the answer.[2] Since this other ground of rejection was not included in the Examiner's answer, we assume that this ground of rejection has been withdrawn by the Examiner.[3] See Ex parte Emm, 118 USPQ 180, 181 (Bd. App. 1957).

Rather than reiterate the viewpoints of the Examiner and Appellant regarding the above-noted rejections, we make reference to the answer (Paper No. 10, mailed July 14, 2000) for the

[2] The Examiner also indicates that Appellant's arguments in the brief have overcome the 35 U.S.C. § 112, first paragraph rejection of claim 1 (answer, page 3).

[3] The appropriate correction should also be made with respect to claim 8, as reflected in the copy of the appealed claims contained in the Appendix to the brief.

Examiner's reasoning, and to the brief (Paper No. 9, filed June 19, 2000) for Appellant's arguments thereagainst.

OPINION

The Examiner relies on figure 23q of Sekiguchi for showing cavity 9b2 formed in a first material (nitride layer 11a) and a second material (oxide layer 20) (final rejection, page 4). However, the Examiner indicates that the conductive layer deposited in the cavity, as shown in Sekiguchi, is not "formed on one dielectric layer while the vertical upper portion[s] are formed on another dielectric" (final rejection, page 5). Relying on figure 2 of Takaishi, the Examiner takes the position that the reference teaches the missing features as polysilicon layer 22 formed on the first material (silicon rich oxide 8) and the upper portion adjoining the second material (oxide 21) (id.).

Appellant argues that Sekiguchi fails to suggest the geometric limitations of claim 1 and especially claim 8, which requires that the cavity upper portion bottom be horizontal compared to upper portion vertical sides (brief, pages 3 & 4). In particular, Appellant points out that cavity 9b2 of Sekiguchi does not have the claimed upper portion bottom and upper portion sides (brief, page 3).

In response to Appellant's arguments, the Examiner acknowledges that "Sekiguchi does not teach the bottom of the conductive layer of the capacitor formed on one dielectric layer while the vertical upper portion[s] are formed on another dielectric" and asserts that Takaishi teaches the missing feature (answer, page 4). The Examiner further compares the claimed cavity shape to the opening shown in figure 4D of Takaishi having a horizontal bottom surface on layer 8 with an upper portion having vertical sides formed by layer 21 and concludes that the combination of the two references teaches the claimed method (id.).

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of presenting a prima facie case of obviousness. See In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993). To reach a conclusion of obvious-ness under § 103, consistent with the holding in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), the examiner must produce a factual basis supported by a teaching in a prior art reference or shown to be common knowledge of unquestionable demonstration. Our reviewing court requires this evidence in order to establish a prima facie case. In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). The

Examiner must not only identify the elements in the prior art, but also show "some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead the individual to combine the relevant teachings of the references." In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

Our review of Sekiguchi confirms that, as conceded by the Examiner, the reference discloses a process for forming contacts in an integrated circuit. However, as depicted in figure 23q, Sekiguchi forms the second material (oxide layer 20) to cover the first material over contact region 4b (nitride layer 11a) after conductive layer 13 is formed in a cavity over the contact region (Col. 25, lines 19-23). Sekiguchi further teaches that contact hole 9b2 is formed by etching the second material layer while nitride layer 11a and nitride sidewall layer 11b function as etch stoppers (Col. 25, lines 23-29). Therefore, Sekiguchi forms a cavity with vertical walls formed of the first and the second material having no bottom of an upper portion. The only bottom portion in Sekiguchi is the top surface of conductive plug 13 that is formed over contact region 4b.

Turning now to Takaishi, we find that the reference relates to a memory cell array in which stacked capacitors are formed in

openings in a second insulating layer and are electrically connected via contact holes of a first insulating layer to impurity doped regions in the substrate (col. 1, lines 49-57). As shown in figure 4B, Takaishi fills contact holes in first insulating layers 8 and 6 with doped polysilicon 22' (col. 4, lines 35-41). Parts of second insulating layer 21 that covers the entire structure are removed to form openings 21a, in which the second insulating layer forms the walls and the first insulating material along with the top surface of plugs 22' form the bottom portion (col. 4, lines 42-50). However, during the step of removing portions of the second insulating layer, contact regions are not exposed since the conductive plugs in the contact holes remain unetched (col. 4, lines 49-50). Although Takaishi forms a conductive layer (polysilicon layer 22) in the opening to conform to the bottom and sides of the opening, the conductive layer does not contact the contact region in the semiconductor material structure since the contact region is covered by plug 22'. Therefore, we disagree with the Examiner's assessment of the teachings in Takaishi as the conductive plug 22' in the contact hole not only does not allow the exposure of the contact region, but also prevents the claimed conductive layer formed in the cavity from contacting the contact region.

We agree with Appellant's assertion (brief, page 3) that the combination of Sekiguchi and Takaishi fails to teach or suggest the specific steps for forming the cavity, as defined in claim 1. As discussed above, neither Sekiguchi nor Takaishi exposes the contact region in the semiconductor material region when portions of the second insulating layer are removed such that the conductive layer formed in the cavity contacts the contact region. In our view, the Examiner's position that the claimed shape of the cavity is formed as Takaishi's conductive layer 22 conforms to the horizontal bottom surface at first insulating layer 8 and the sides defined by second insulating layer 21 (answer, page 4), is inconclusive because neither reference teaches or suggests the steps of exposing and contacting the contact region. Thus, assuming, arguendo, that it would have been obvious to combine Sekiguchi and Takaishi, as held by the Examiner, the combination would still fall short of teaching or suggesting the claimed removing portions of the layer of the second material and exposing the contact region and forming a cavity having the shape, as recited in claim 1.

In view of our analysis above, we find that the Examiner has failed to set forth a prima facie case of obviousness with respect to claim 1 because the necessary teachings and

suggestions related to the claimed step of removing portions of the layer of the second material and forming the specifically shaped cavity exposing the contact region, as recited in independent claims 1 and 8, are not shown. Accordingly, we do not sustain the 35 U.S.C. § 103 rejection of independent claims 1 and 8, nor of claims 2-7 and 9-16 dependent thereon.

CONCLUSION

In view of the foregoing, the decision of the Examiner to reject claims 1-16 under 35 U.S.C. § 103 is reversed.

REVERSED

KENNETH W. HAIRSTON Administrative Patent Judge	)	
ANITA PELLMAN GROSS Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
MAHSHID D. SAADAT Administrative Patent Judge	)	

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Texas Instruments Incorporated
P.O. Box 655474, M/S 3999
Dallas, TX 75265